

Smart Cut™ Nano Technology

Dr. Carlos Mazuré
CTO, Soitec
Chairman, SOI Industry Consortium

➤ **European Innovation Day**
Tokyo, October 15, 2018



soitec



Agenda

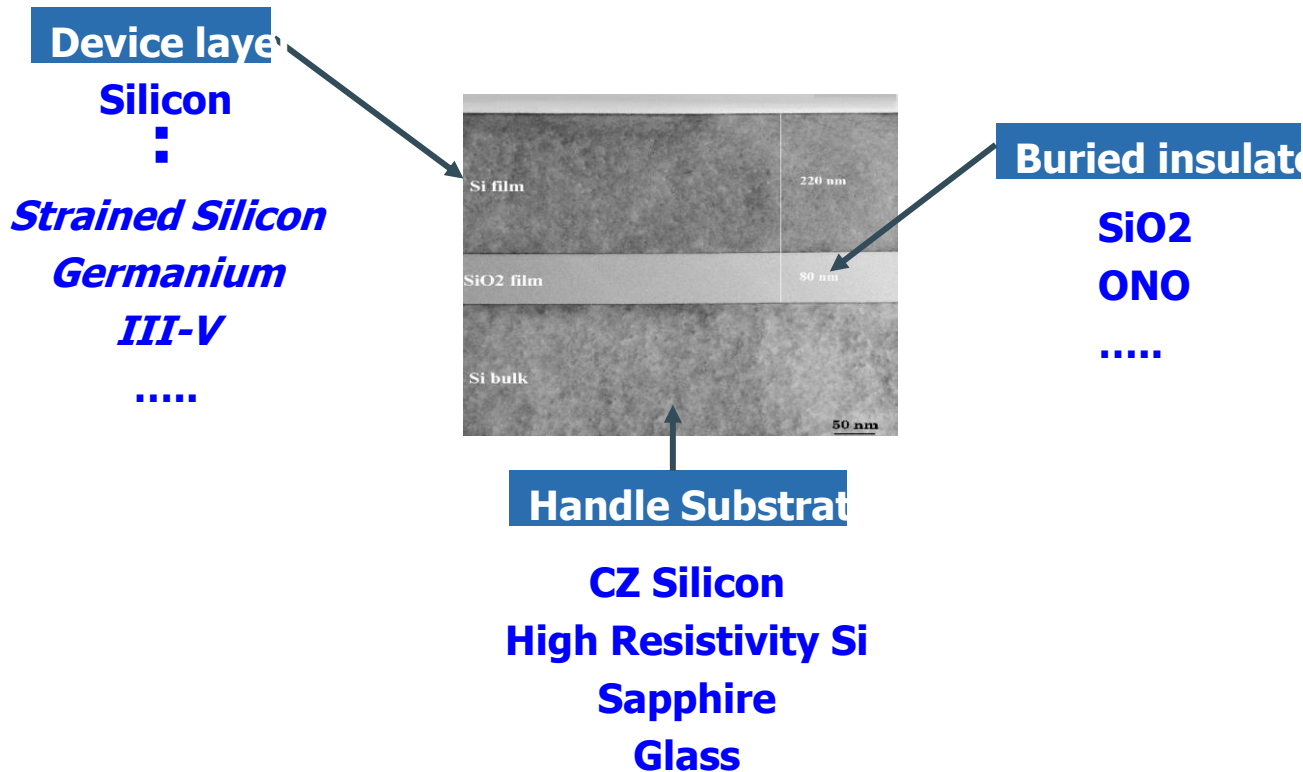
A Introduction

B RF

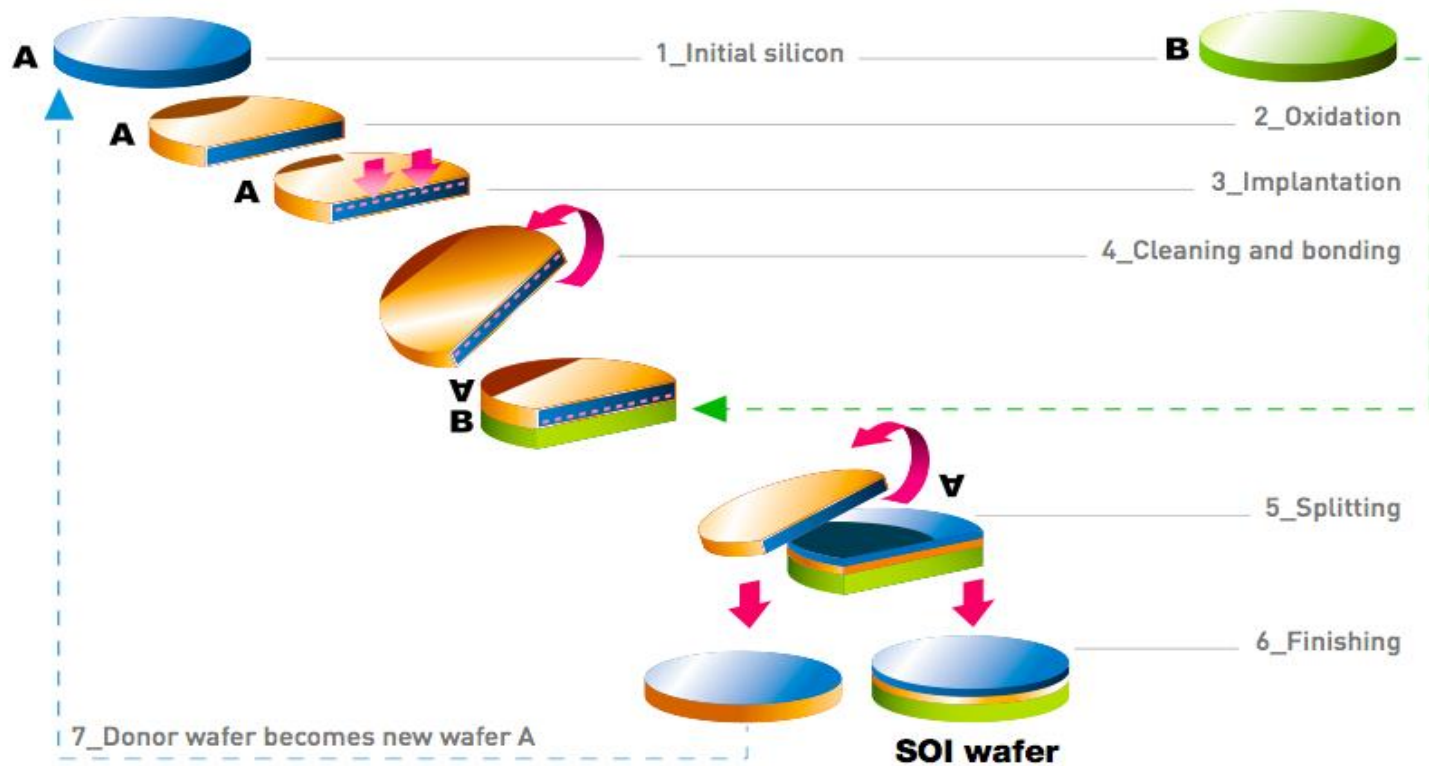
C MEMS

D Takeaways

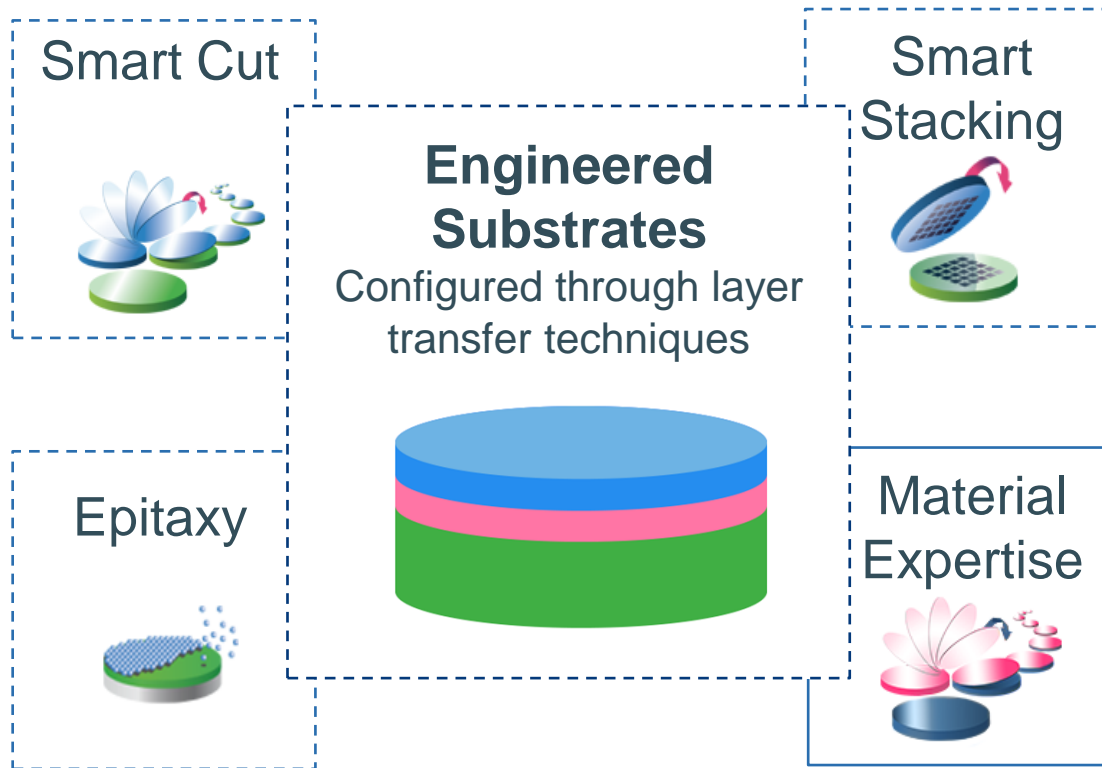
Substrate Engineering: Built-in Functionality



Smart Cut™ Technology

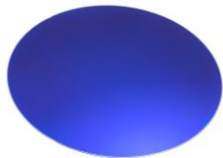


3 core technologies available and material expertise to manufacture engineered substrates

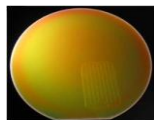


Smart Cut Flexibility

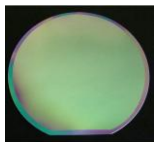
Material Options



Silicon On Insulator



Silicon On Sapphire



Piezzo On Insulator



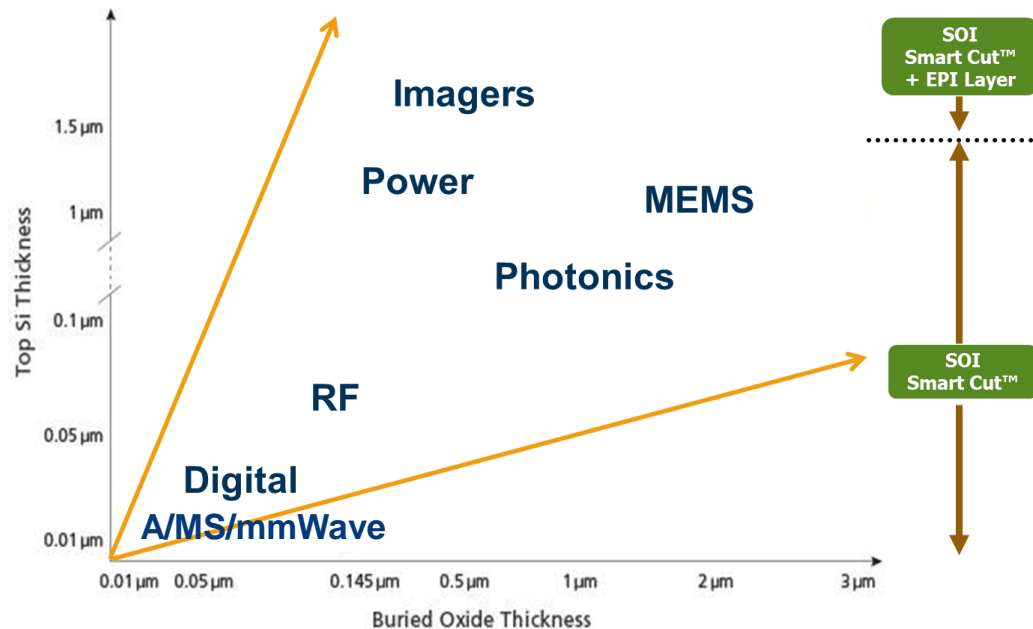
InGaN On Sapphire



InP On GaAs

...

Thickness Capabilities



Soitec in the Value Chain

Engineered substrates

soitec



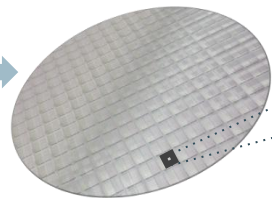
*Smart Cut™
technology*



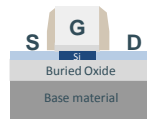
*SOI substrates
(Silicon on Insulator)*



*Starting
wafers*



*SOI processed
wafer
with multiple raw dice
per wafer*



SOI transistor



*Silicon die
with millions of
transistors*



IC



PCB



Our engineered substrates are at the heart of everyday life

Data Centers

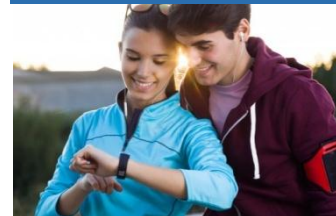


**Outstanding
Performance**



Longer battery life

IoT



**Soitec's
engineered
substrates**



**Higher
reliability**



Optimized cost

Automotive

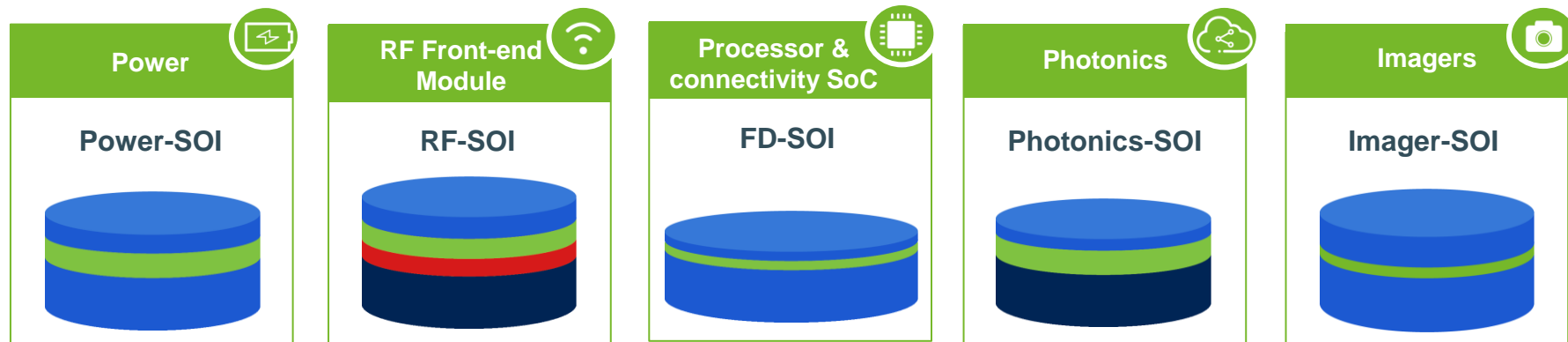


Smartphones



Soitec – A Leading Engineered Substrates Supplier addressing Large Consumer related Markets

In Production





Agenda

A Introduction



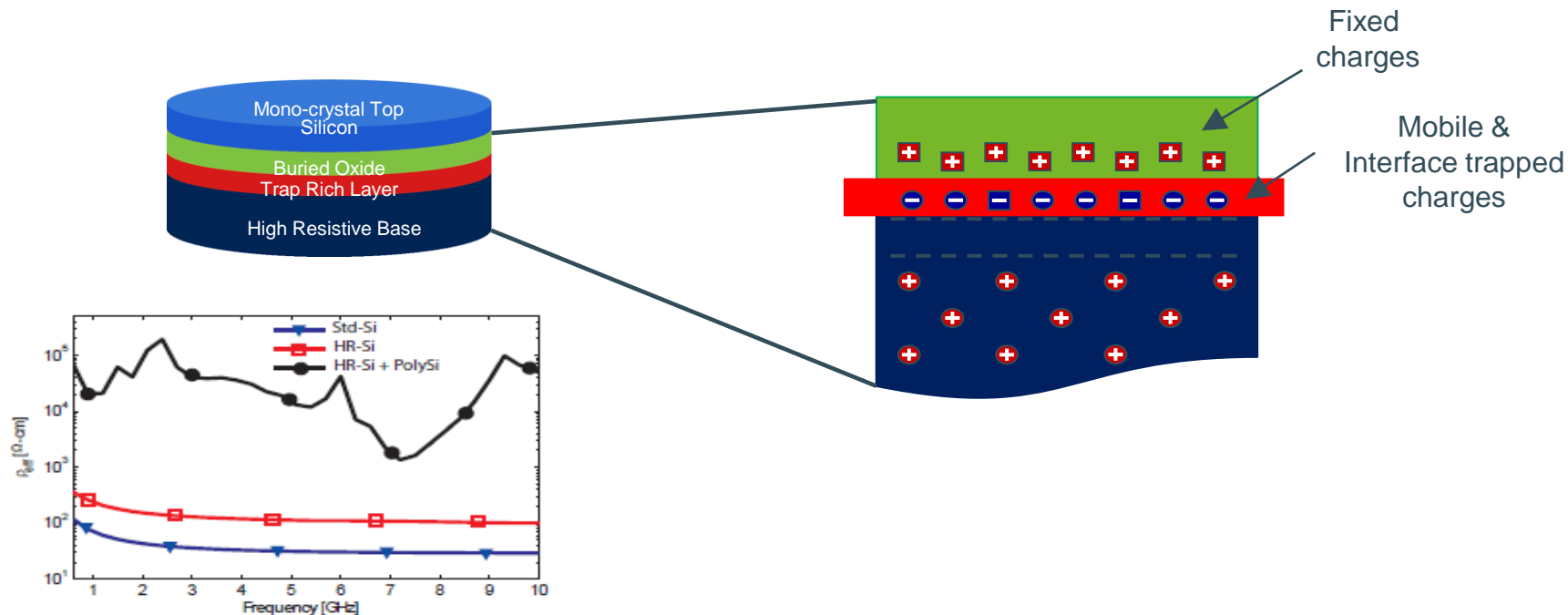
B RF

C MEMS

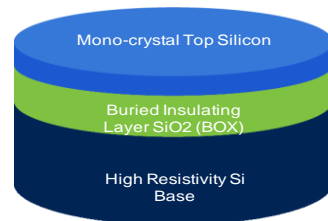
D Takeaways

Enhanced Signal Integrity SOI - RFeSI™

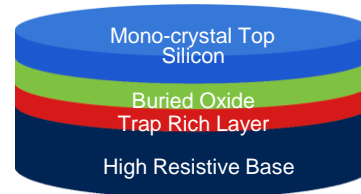
Trap Rich layer freezes the highly conductive layer at BOX – Handle interface



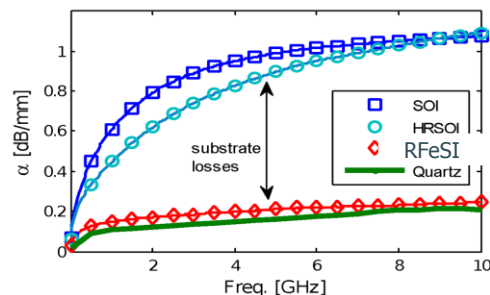
RFeSI™ addresses all FEM challenges



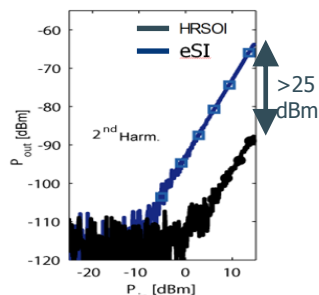
HR-SOI



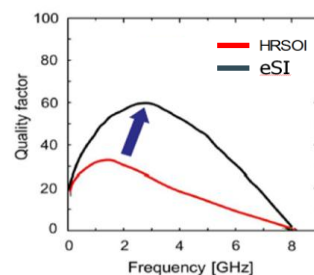
RFeSI SOI



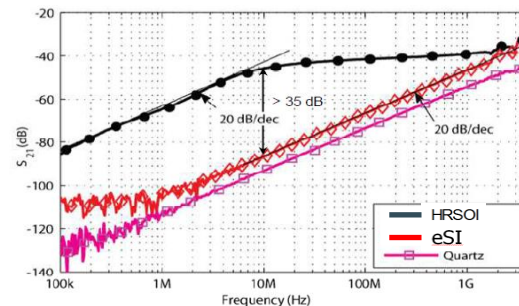
Insertion Loss



Linearity



High Q passives

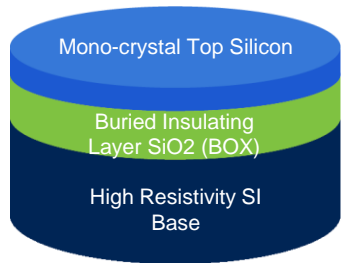


Crosstalk

Source: UCL

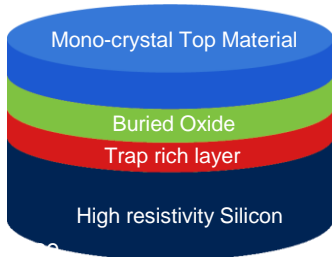
Soitec RF-SOI wafers : HRSOI & RFeSI™

HRSOI



RFeSI Enhanced Signal Integrity

RFeSI relies on a unique Trap Rich layer that will limit high frequency signal propagation in the substrate boosting device RF performance



Manufacturing in 200mm and 300mm



Bernin 1



Bernin 2



Simgui



Singapore



Value proposition

PERFORMANCE

- › Higher Linearity
- › Lower RF losses
- › Lower crosstalk
- › High quality passives



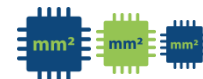
COST

- › Lower than GaAs and MEMS
- › Integration with switch, amplifiers and passives
- › Available in 200/300mm

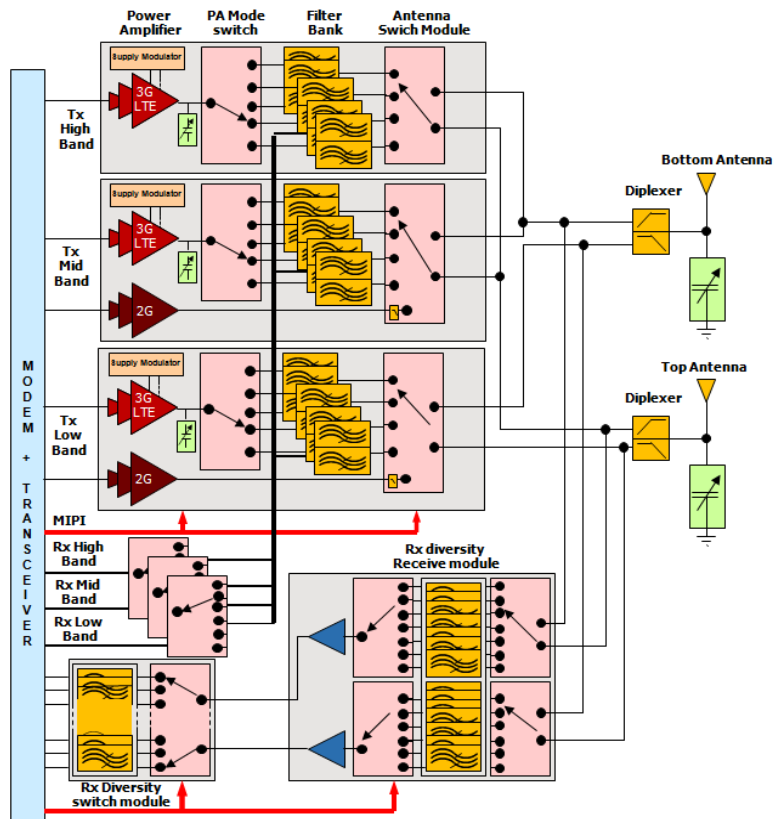


AREA

- › Lower die size



4G and 5G sub <6GHz Front End Module



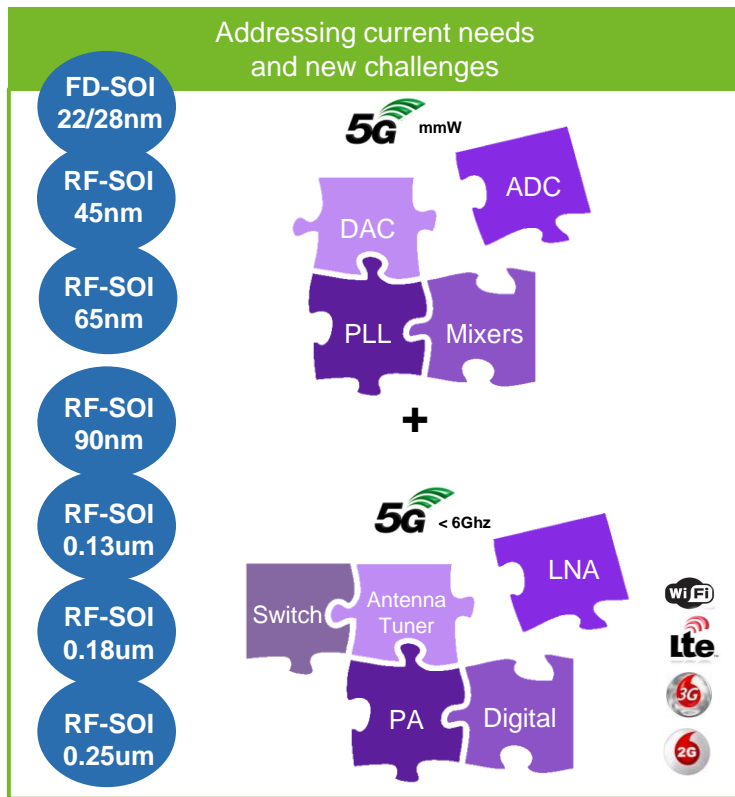
Switch	 	RF-SOI	✓
Antenna tuner	 	RF-SOI	✓
Diplexer	 	RF-SOI	✓
LNA	 	RF-SOI	✓
PA	 	RF-SOI	✓
Filters		Piezo On Insulator	✓

RF-SOI Innovation: From R&D to Tech Dev to Mfg



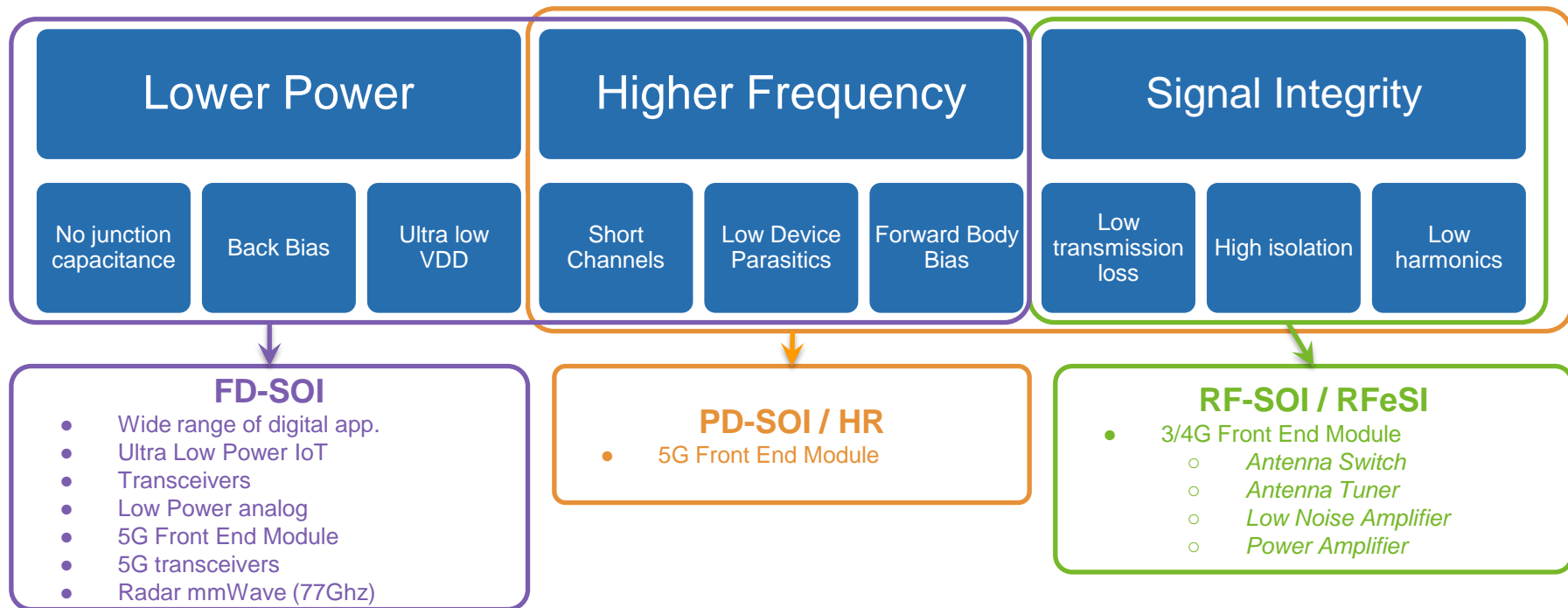
Contribution of many organizations and companies

Strong SOI ecosystem driving innovation for 4G/5G



SOI mixed signal platforms for 4G & 5G

Mixed signal design & integration options



RF-SOI Innovation: From R&D to Tech Dev to Mfg



Workshop Agenda

08:00 - 09:00 Registration

Session 1: Opening Remarks

09:00 - 09:08 Xi Wang, Director General of Shanghai Institute of Microsystem and Information Technology
09:08 - 09:15 Carlos Mazure, Chairman and Executive Director, SOI Industry Consortium

Session 2: Keynote Speech

09:15 - 09:40 **Join Hands with Industry Partners - Hop on the 5G Shuttle Together**
Danni Song, Project Manager, China Mobile
09:40 - 10:05 **Riding the 5G Silicon Wave: How Advances in 5G Radio Architectures Benefit from RF-SOI**
Michael Reiha, Head of RFIC R&D, Nokia Mobile Networks
10:05 - 10:30 **RF-SOI Enabling the RF Wireless Front End: History, Future and Challenges**
Julio Costa, Director of Technology Development, Qorvo

10:30 - 11:00 Break *sponsored by*



SOI Industry Consortium 1.0: Accelerator of ecosystem development

› Ecosystem focused workshops around the world

- › Oct 2009, @ IMEC, Leuven, Belgium
- › Sept 2010, @ Univ of Tokyo, Japan
- › Dec 2010, San Francisco, US
- › April 2011, Hsinchu, Taiwan
- › Feb 2012, San Francisco, US
- › Dec 2012, San Francisco, US

› Topics: technology, modeling and fabless requirements

› Contributors: academia, R&D (Institutes, Industry), EDA, Fabless

SOI Industry Consortium 2.0:

Ecosystem growth and promote adoption

- › Industry events for the industry by the industry around the world
 - › Sept 2014, Shanghai
 - › Jan 2015, Tokyo; Feb 2015, Si Valley; April 2015, Hsinchu, Taiwan; Sept 2015, Shanghai
 - › Jan 2016, Tokyo; April 2016, Si Valley; Sept 2016, Shanghai
 - › April 2017, Si Valley; Jun 2017, Tokyo; Sept 2017, Shanghai
 - › *Mar 2018 Brussels; April 2017, Si Valley; Jun 2018, Tokyo; Sept 2018, Shanghai*
- › Topics: foundry platform, design ecosystem and first products
- › Contributors: Institutes, Industry, Fabless, Market Analysts, Investment Funds

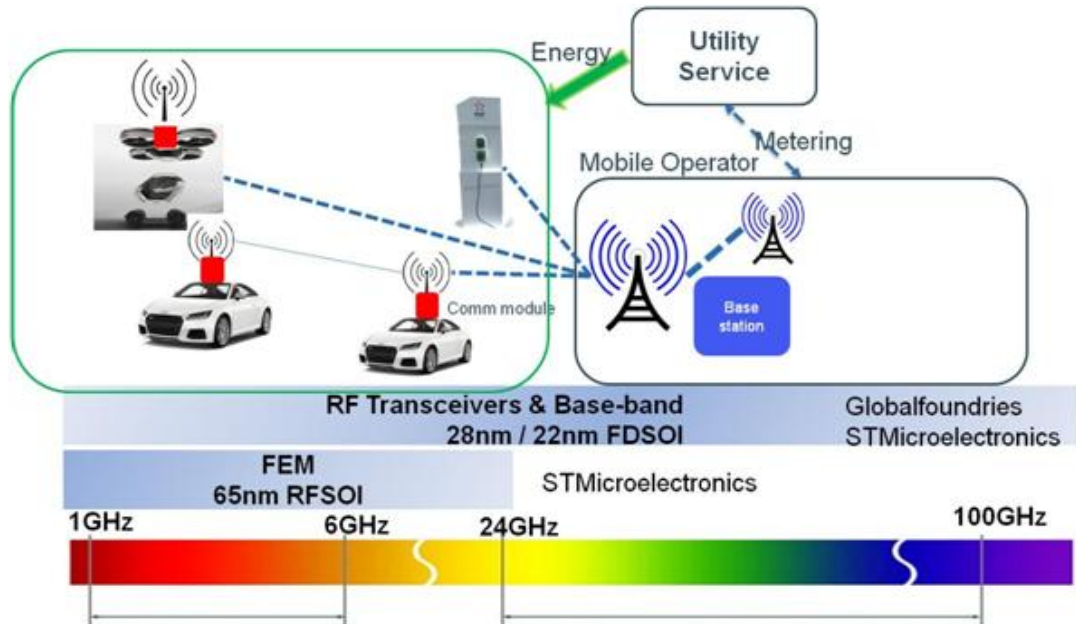
ELEMENT5 Ecosystem Partnership: 5G connectivity

Main challenges and DRIVERS

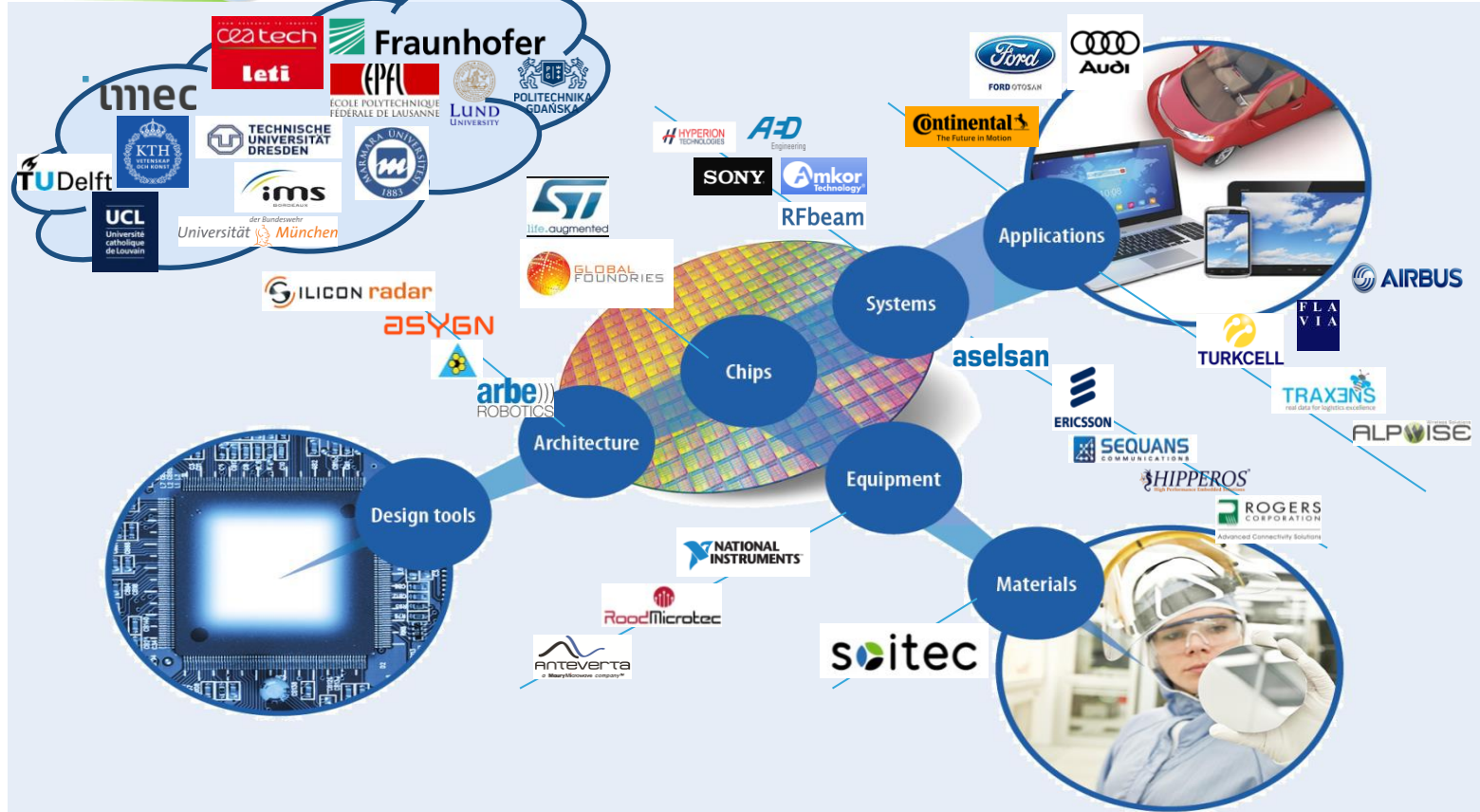
- Increased linearity and higher number of communication bands and bandwidth
- Robust and **highly integrated RF FEM** with **no performance degradation at high temp**

Driving demand:

- Reliable **cyber-physical communication systems (V2X)** for Smart Autonomous Vehicles (**Automotive, Aeronautics**) (communication modules & equipments)
- Low-latency, available, low-power **Infrastructure** (communication modules & equipments)
- New business models with mobile connectivity for utility providers (**Energy, Smart Metering**)



ELEMENT5 Ecosystem Partnership: Value Chain





Agenda

A Introduction

B RF

C MEMS

D Takeaways



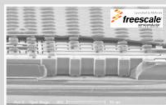
SOI for Sensors – MEMS - NEMS

FROM MICROELECTRONICS TO NANOTECHNOLOGY
cea tech

MEMS SENSORS FOR MTM

Leti

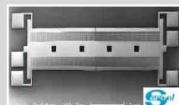
Inertial sensor



3-axis Accelerometer



3-axis Gyroscope

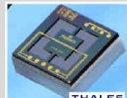


Geophone

Pressure sensor



Capacitive pressure sensor

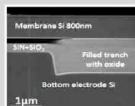


Piezoresistive pressure sensor



3-axis force sensor

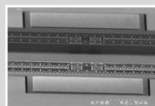
Acoustic sensor



cMUT

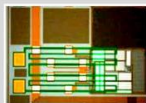


Microphone

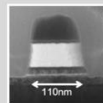


Microphone

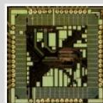
Magnetic sensor



Above-IC GMR sensor



TMR sensor and resonator



3-axis Compass

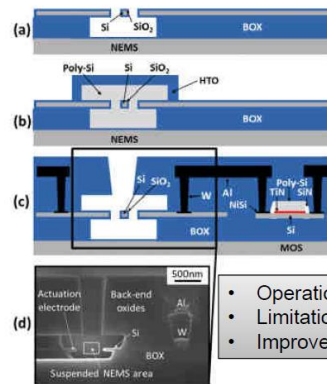
7

FROM MICROELECTRONICS TO NANOTECHNOLOGY
cea tech

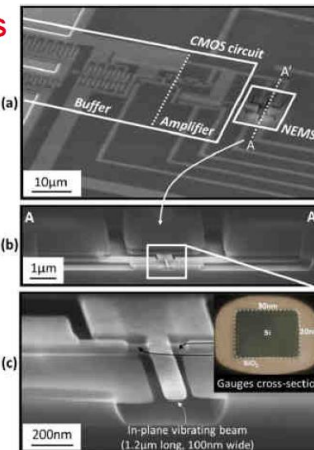
MEMS AT THE HEART OF CMOS SOI

Leti

MONOLITHIC INTEGRATION NEMS IN SOI CMOS



- Operation at high freq. (100Mhz)
- Limitation of parasitics
- Improvement of SNR



From J. Arcamone, Nanotechnology 25 (2014) 435501

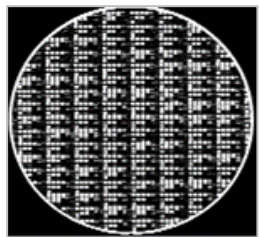
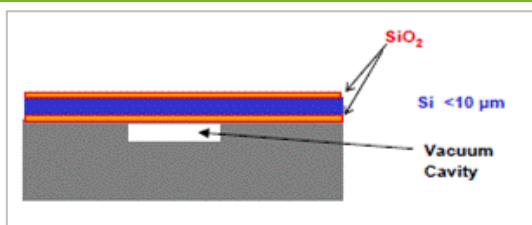
→ New opportunities in NEMS-based mass spectrometry or hybrid NEMS/CMOS logic

20

Source: Presented at Tokyo SOI Workshop, June 2016

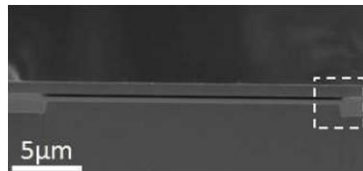
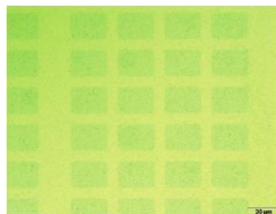
SOI for Sensors & Actuators: Layer transfer on cavities

“Thick”
5-10 μm

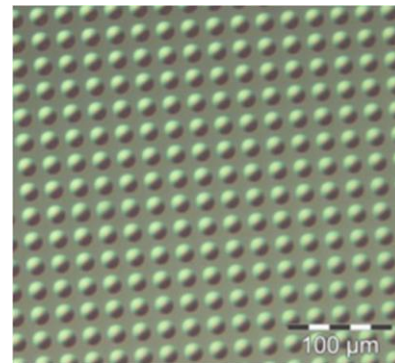


25-100-500 μm

“Thin”
 $\sim 1 \mu\text{m}$



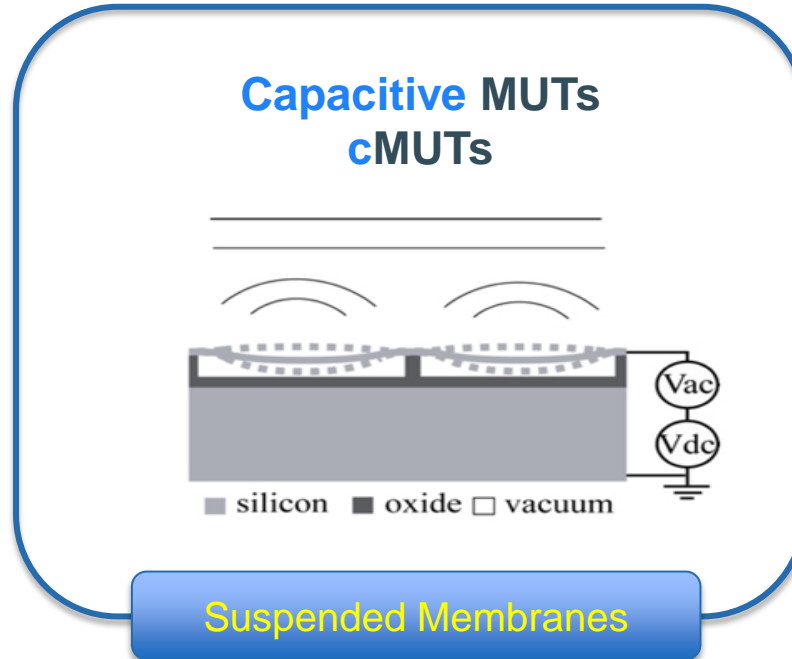
“Ultra-Thin”
 $\sim 0.15 \mu\text{m}$



OKMETIC

cMUTs & pMUTs

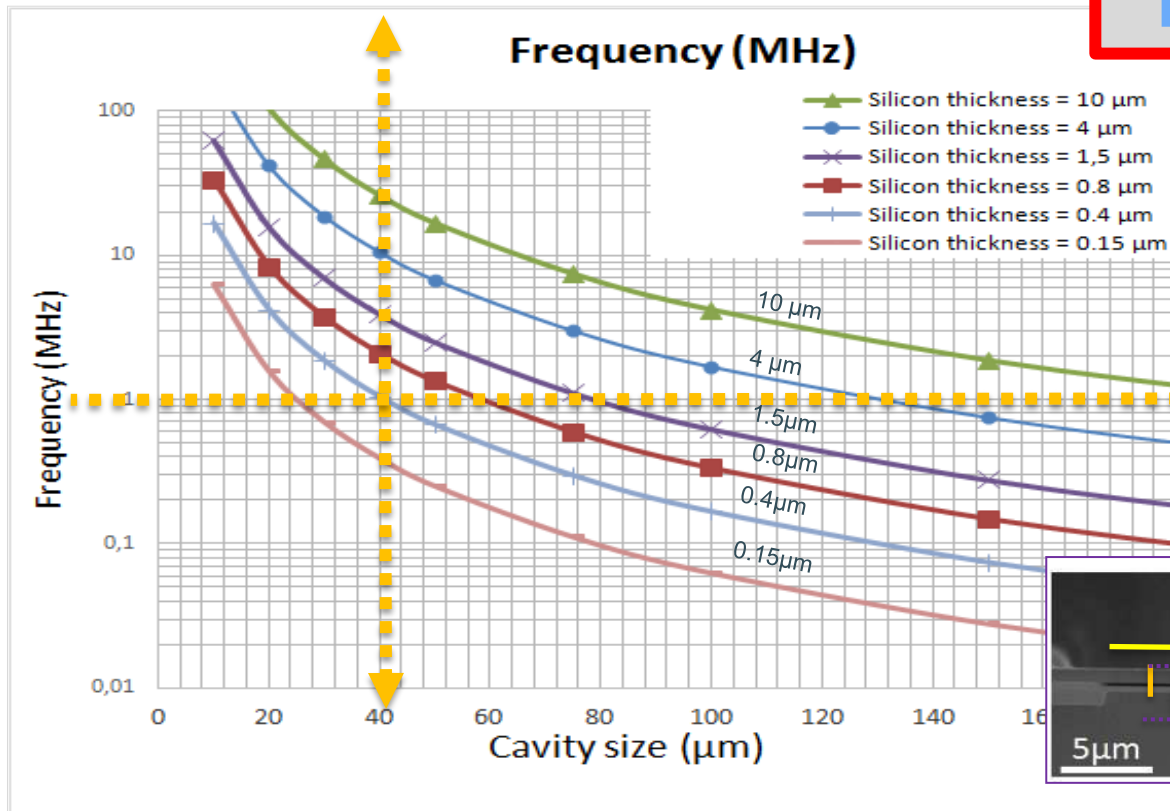
(Micromachined **U**ltrasonic Transducers)



MUT: Resonance Frequency control (very simplified model*)

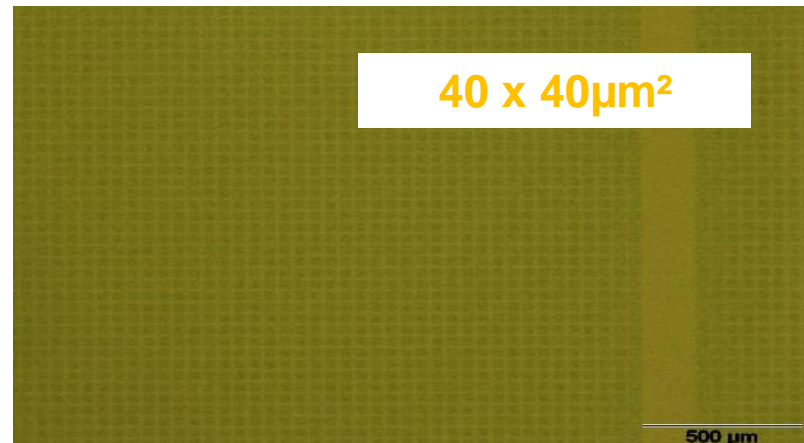
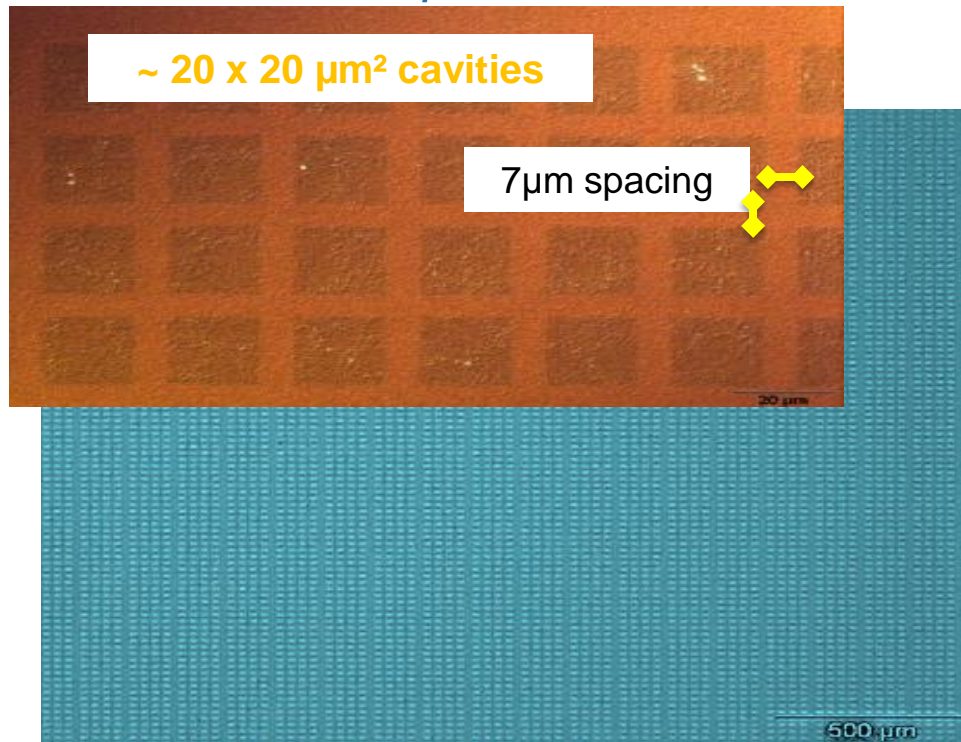
$$F_{\text{res}} \propto t / w^2$$

(*) Not including :
- stress effects,
- damping, loading,
- DC polarization
- electrode stack
- etc ...



Si membranes on cavities :

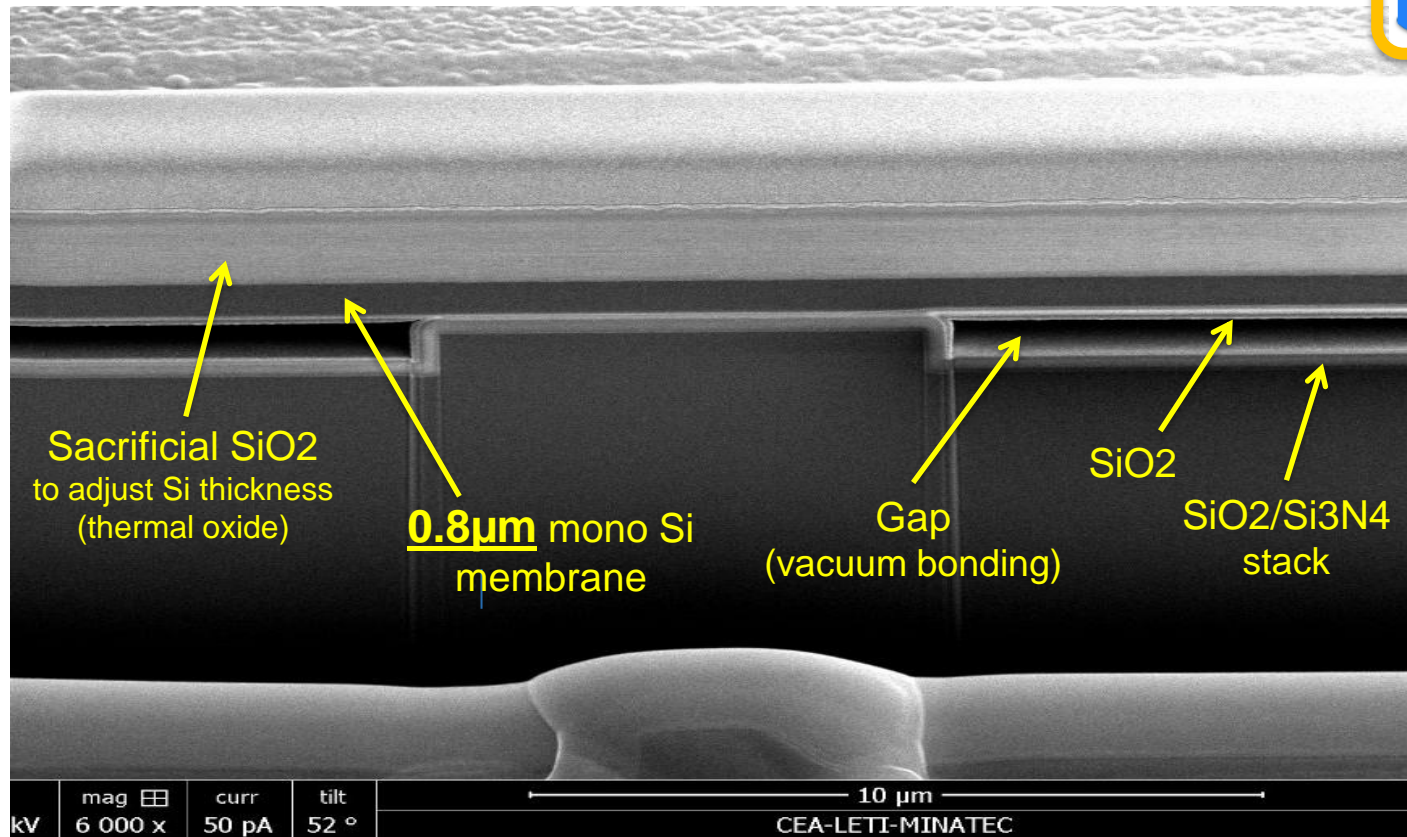
- $20 \times 20 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$ cavity arrays
- $\sim 1 \mu\text{m}$ Si membrane



Wafer diameter : 200mm

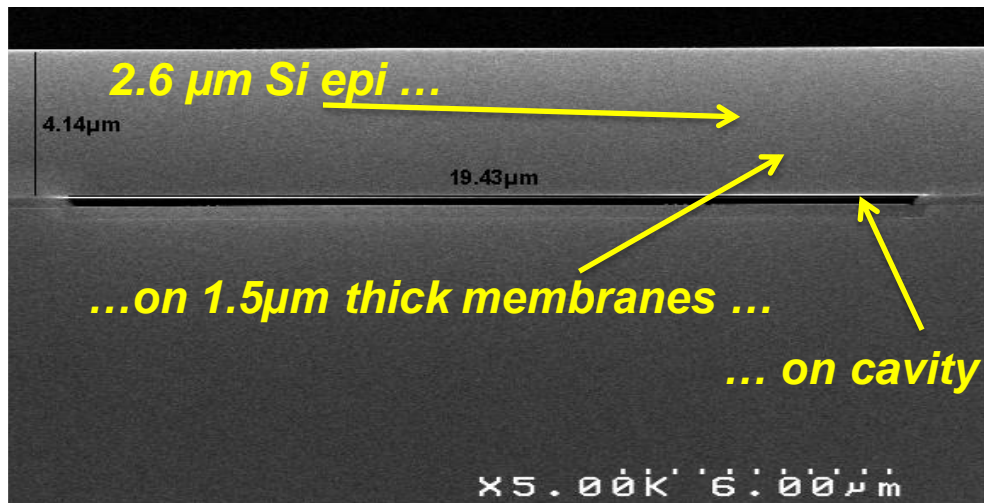
➔ Very dense arrays
become possible !

0.8 μm thin membranes on 40 x 40 μm^2 arrays



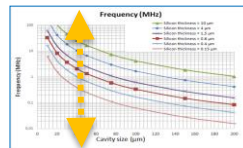
~ 4 μm epi thickened membranes on 20 x 20 μm^2 arrays

Front-end CMOS
compatible
engineered substrate



Membrane Thickness flexibility

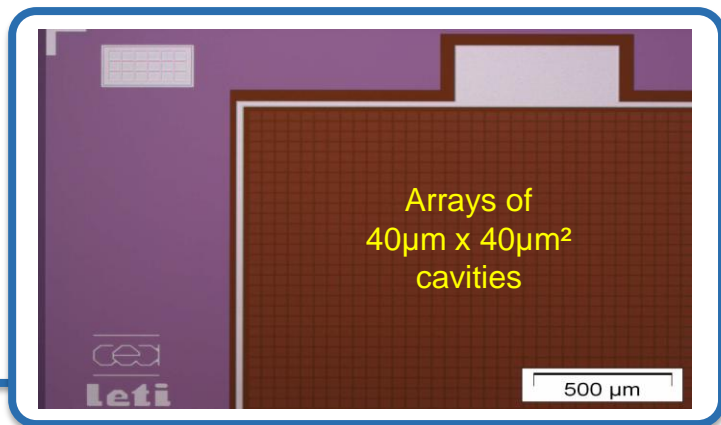
- Tuning downwards by etching, sacrificial oxidation,...
- Tuning upwards by epitaxy (before or after transfer on cavity)



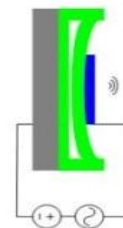
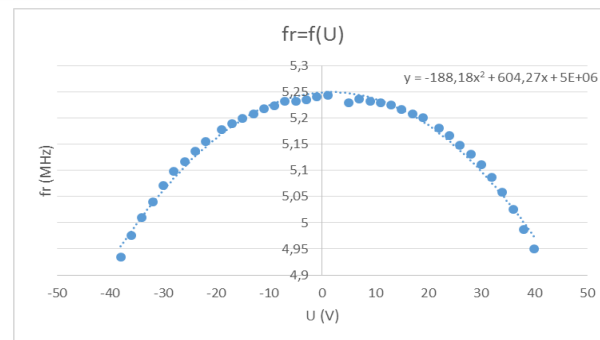
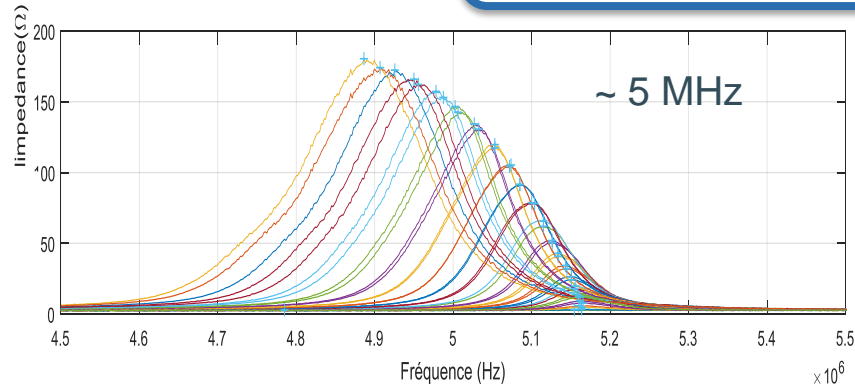
Collaboration



cMUT electrical characterization



Collaboration



More than Moore: Ecosystem growth

2018 Japan SOI Workshop Tokyo, 2018.10.26

Takeda Hall, Tokyo University

Session: Keynotes

Chair: **Carlos Mazure, SOI Industry Consortium**

9:40 - 10:10 Distributed AI and computing at edge and nodes for sensors, Giorgio Cesana, Sr. Director, STMicroelectronics

10:10 – 10:40 RF- & FD-SOI: addressing substrate supply to support accelerated growth, Jean-Marc LeMeil, Director, Soitec

10:40 – 11:10 FD-SOI for ultra low power edge computing, Jon Cheek, Director, NXP

Session: MEMS & Sensors

Chair: **Jon Cheek, NXP**

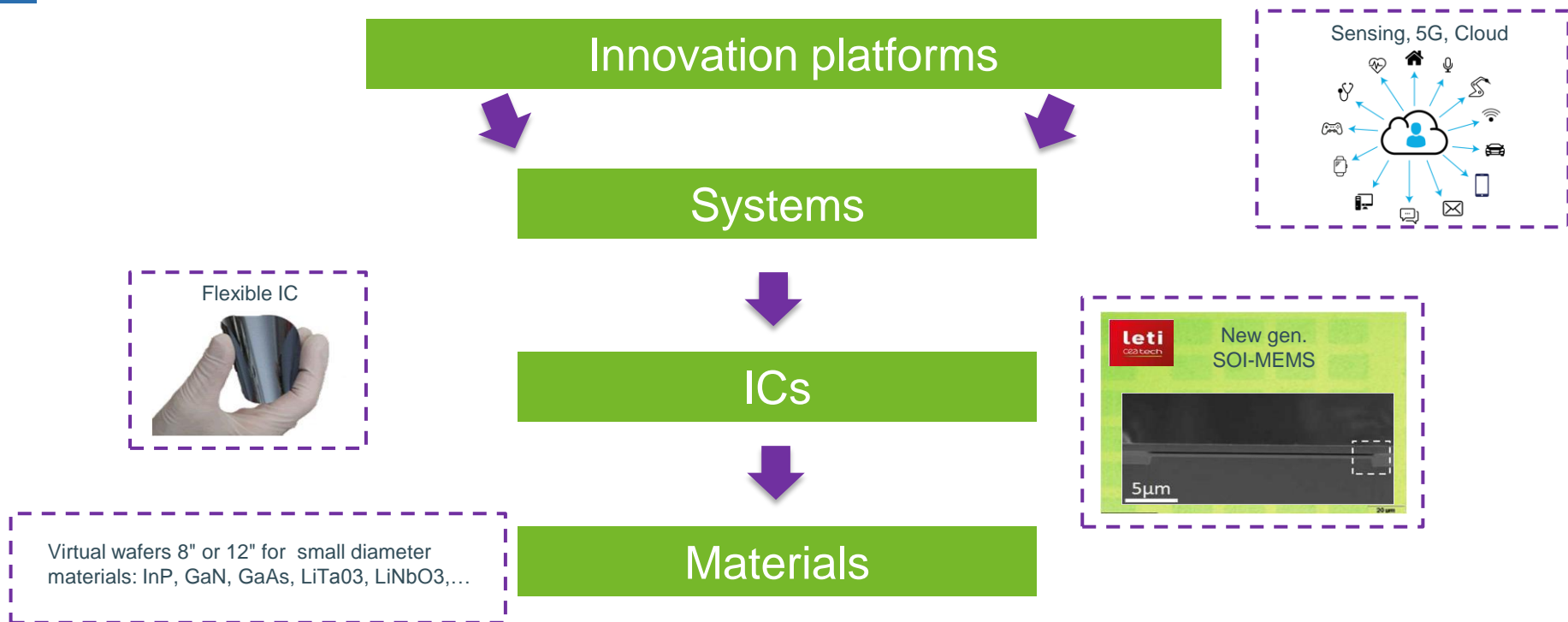
11:40 - 12:05 A Time-of-Flight Range Image Sensor with High Near Infrared Quantum Efficiency Using SOI-Based Fully-Depleted-Substrate Detectors; Prof. Shiji Kawahito, Shizuoka University

12:05 – 12:25 An Overview of SOI based MEMS; Jean-Philippe Polizzi, MEMS Business Development Manager, Leti-CEA

12:25 – 12:50 Smart Cut technology applied to MEMS: illustration in the field of ultrasonic transducers; Bruno Ghyselen, Sr. Expert, Soitec

12:50 - 13:50 Lunch

Takeaway: Substrate-Device-Application Co-Optimization





Disclaimer

© Exclusive property of Soitec. This document contains confidential information. Disclosure, redisclosure, dissemination, redissemination, reproduction or use is limited to authorized persons only. Disclosure to third parties requires a Non Disclosure Agreement. Use or reuse, in whole or in part, by any means and in any form, for any purpose other than which is expressly set forth in this document is forbidden.